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Sampling for Oscilloscopes and Other RF Systems: Dc Through X-Band

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Abstract—Sampling techniques as used in wideband oscilloscopes have, in the past, yielded bandwidths up to 4000 MHz. This approach has now been employed to achieve bandwidths in excess of 15 GHz. The design requirements necessary for this extended bandwidth are presented along with a detailed description of one solution to the design problem.

The device is basically a two-diode sampler located at the center of a dielectric filled, biconical cavity containing the RF transmission line. The RF line is perpendicular to the axis of the biconical cavity. The sampling pulse is introduced into the cavity by applying it directly between the centers of the opposite faces of the cavity. This establishes a potential difference between two points on the ground conductor of the RF transmission line being sampled. This technique is basic to the operation of the device and plays a key role in the reduction of sampling loop inductance, which would limit the bandwidth. The equivalent circuits are presented along with the appropriate defining equations. The relationship between bandwidth, input VSWR, and step response overshoot, are presented, along with the typical measured results.

Introduction

SAMPLING TECHNIQUES have long been used on periodic waveforms to achieve wide bandwidths in oscilloscopes [1]–[12]. The same technique has been used in phase-locked loops [13], in random sampling voltage detectors, and other RF systems. Although the applications of sampling are quite different, the basic requirements for a broadband sampling device are nearly the same regardless of the application. This technique has now been extended to X-band frequencies and above by the development of a sampling device with a bandwidth in excess of 12.4 GHz.

There are other performance characteristics to be considered when evaluating a sampling device. Several of these are input signal dynamic range, sensitivity, input voltage standing-wave ratio, phase response, and mechanical configuration. The bandwidth of such a device, however, is the most important single performance characteristic.

There are many electronic systems presently using sampling devices and these devices vary widely in performance and general configuration. The state-of-the-art in wideband sampling devices up to now has been the 4 GHz bandwidth presently available in sampling oscilloscopes [14].

The bandwidth of a sampling device employing semiconductor diodes is determined entirely by the diodes, by the sampling pulse and by the method used to connect them to the RF transmission line being sampled. This paper will discuss these basic elements and the design requirements for each. A unique sampling circuit will be presented along with its mechanical realization. Typical measured performance data will then be presented, completing the design cycle.

A. Basic Sampling Requirements

Figure 1 shows an idealized sampling circuit. Switch S is closed for a short period of time, allowing the sampling capacitor C to charge to some fraction of the voltage

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appearing at the input. The switch is then opened, leaving the sample of the input stored on the sampling capacitor. The ratio of the resulting capacitor voltage e_{sample} to the voltage appearing at the input e_{in} is a measure of the efficiency of the sampling circuit. This assumes that the voltage on the sampling capacitor is reset to zero before each new sample. The sampling efficiency is, therefore, defined as follows:

$$\eta = \frac{e_{\text{sample}}}{e_{\text{in}}} . \tag{1}$$

The bandwidth of the device is defined to be the frequency at which η is $1/\sqrt{2}$ times its dc or low-frequency value. The first zero in the frequency response of such a device occurs when the time for which the sampling gate is closed equals the period of one cycle of the input CW signal.

Consider the general two-diode sampling circuit shown in Fig. 2. A two-diode configuration will be considered, since it provides isolation between the sampling pulse and the input signal line. The input transmission line is shown in a feedthrough form, although, for this analysis, it could also be terminated with a 50 ohm resistor at the sampling point.

The diodes are normally back biased and are gated in a balanced fashion such that a low impedance path is provided through the diodes and the sampling capacitors to ground. The sampling capacitors charge towards the voltage appearing at the input. The diodes are then returned to their normal back-biased condition. The bandwidth of the sampling device is inversely proportional to the time for which the diode impedance is low. This time interval is normally called the gate width and will be designated by t_g. Figure 3 shows the diode bias and sampling pulse which yield the gate width t_g. It can be shown that the bandwidth of a sampling device is approximately [15]

$$B_W(\text{GHz}) \cong \frac{350}{t_g(ps)} . \tag{2}$$

This assumes that the device has zero or small overshoot, a Gaussian frequency roll off, and a linear phase over the passband. It should be noted that a bandwidth of 12.4 GHz corresponds to a t_g of approximately 28 picoseconds.

The sensitivity of the sampler, analogous to conversion loss in a mixer, is determined by the efficiency of charge transfer from the input transmission line to the sampling capacitors. Ideally, we would like the diode impedance to be equal to zero during the time t_g. This would allow the sampling capacitor to charge to a larger fraction of the input voltage, increasing the sampling efficiency. In practice, however, the diode impedance remains relatively high with respect to its series resistance R_s.

The circuit of Fig. 2 can be simplified by considering separately the input sampling circuit and the diode gating circuit. Using the diode equivalent circuit shown in Fig. 2, the equivalent input sampling circuit can be reduced to that shown in Fig. 4. Here, both diodes have been combined into one. This approximation is consistent with a small signal analysis. The RF transmission line behaves as a voltage generator with internal impedance $Z_0/2$. The circuit element values shown in Fig. 4 are given in terms of the diode equivalent circuit element value as follows:

$$L_1 = L_s/2 \tag{3}$$

$$R = R_s/2 \tag{4}$$

$$R_1 = R_j/2 \tag{5}$$

$$C = 2C_j \tag{6}$$

$$C_1 = 2C_s \tag{7}$$

$$C_2 = 2C_p. \tag{8}$$

The inductor L_2 represents any added inductance in the connection between the ground of the input transmission line and the ground of the sampling pulse generators. The sampling pulse generator impedance is represented by R_{s_g}.

The circuit of Fig. 4 can be further simplified by assuming that C_2 can be masked out as will be shown later. Also, C_1 can be replaced by a short circuit since $C_1 \gg C$. Assuming that R_{s_g} is included in R and combining L_1 and L_2, the circuit can be redrawn as shown in Fig. 5. The effects of the sampling pulse have been neglected here and will be considered separately later.

If we now compute the voltage V_{d_s}, which results from the application of an input signal e_{in}, the resulting equation defines the bandwidth of this portion of the circuit.

$$V_{d_s} = \frac{e_{\text{in}}\left[\frac{1}{LC}\right]}{s^2 + s\left[\frac{1}{CR_1} + \frac{R + Z_0/2}{L}\right] + \left[\frac{R + Z_0/2}{R_1CL} + \frac{1}{LC}\right]} . \tag{9}$$

Normally

$$\frac{1}{CR_1} \ll \frac{R + Z_0/2}{L} \tag{10}$$

and

$$\frac{R + Z_0/2}{R_1CL} \ll \frac{1}{LC} . \tag{11}$$

These simplifying assumptions reduce (9) to the following:

$$V_{d_s} = \frac{e_{\text{in}}\left[\frac{1}{LC}\right]}{s^2 + s\left[\frac{R + Z_0/2}{L}\right] + \left[\frac{1}{LC}\right]} . \tag{12}$$

Let us now consider the equivalent sampling pulse circuit shown in Fig. 6. The equivalent circuit element values are related to the diode parameters as follows:

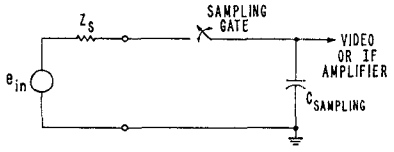

Fig. 1. Idealized sampling gate.

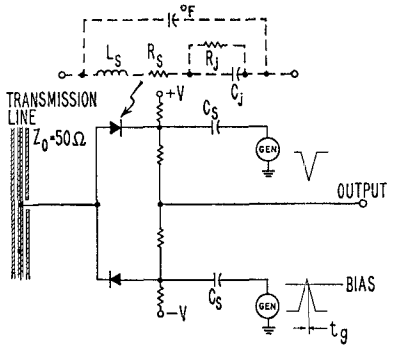

Fig. 2. General two-diode sampling circuit.

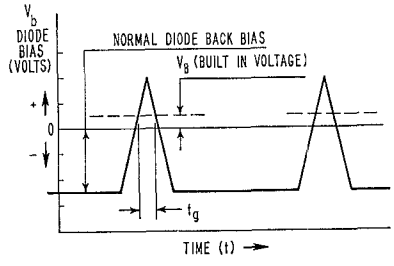

Fig. 3. Diode bias and sampling pulse.

$$R = 2R_s \tag{13}$$

$$R_1 = 2R_j \tag{14}$$

$$C = C_j/2 \tag{15}$$

$$L = 2L_s. \tag{16}$$

As in the case of the input equivalent circuit, C_s and C_p have been neglected. If we write the equation for the voltage, which appears across the diode junction V_{d_p}, in terms of the available sampling voltage E_p, we obtain the following equation:

$$V_{d_p} = \frac{E_p\left[\frac{1}{LC}\right]}{s^2 + s\left[\frac{R + Z_s/2}{L}\right] + \left[\frac{1}{LC}\right]}. \tag{17}$$

Equations (12) and (17) are exactly the same except for the driving voltages. This is not unexpected, since two equal RLC networks connected in series have the same bandwidth as determined by the complex pole locations as the parallel combination of the same two networks. (This assumes that they are both driven by a zero impedance source.)

The fact that the R, L, and C limitations, as set by the input sampling equivalent circuit, are the major factors controlling the bandwidth of the device can be seen by considering the idealized sampling pulses as

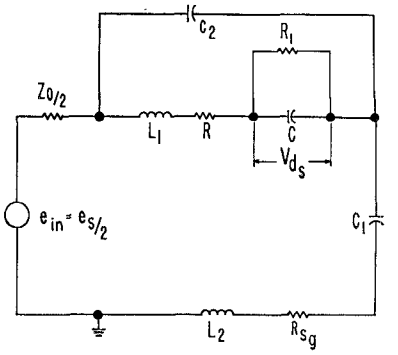

Fig. 4. Equivalent input sampling circuit.

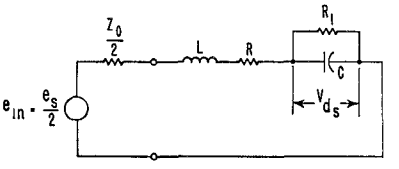

Fig. 5. Simplified input sampling circuit.

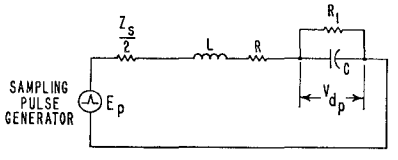

Fig. 6. Equivalent sampling pulse circuit.

shown in Fig. 7. Given the gate time t_g, the contour of the pulse above the bias line A only affects the diode impedance and thereby the sensitivity of the sampling device, that is, the amount of charge transferred from the input transmission line to the sampling capacitors in one sample. Ideally, we would like a square pulse above the bias line A to give maximum sensitivity. The bandwidth, however, will be relatively unchanged as long as the gate time is fixed. It should be noted that the risetime of the sampling pulse can be much greater than the gate time t_g.

The pole locations of (12) will determine the bandwidth over which the circuit will operate. If we want the response of the device to a perfect input voltage step to have less than a given overshoot, we can achieve this by insuring that the voltage appearing across the diode junction as a result of the voltage step input has less than the same amount of overshoot. For those applications of sampling which require an accurate real time response, the typical overshoot objective for the system is 5 percent. Using the standard notation, we can rewrite (12) as follows:

$$V_{d_s} = \frac{e_{in}\left[\frac{1}{LC}\right]}{s^2 + s\left[\frac{R + Z_0/2}{L}\right] + \left[\frac{1}{LC}\right]} = \frac{e_{in}[\omega_n^2]}{s^2 + s2\delta\omega_n + \omega_n^2} \tag{18}$$

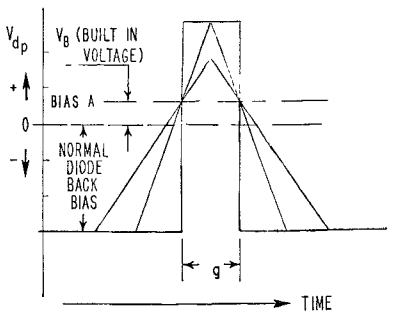

Fig. 7. Idealized sampling pulses at diode junction.

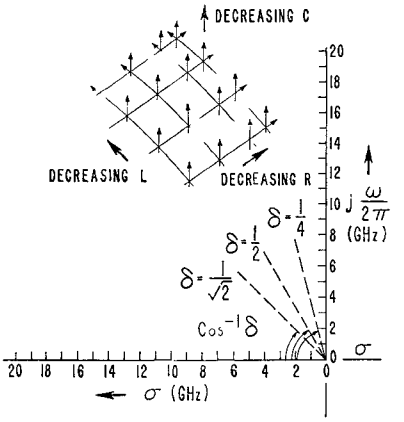

Fig. 8. Sampling circuit pole locations.

$$\omega_n = \frac{1}{\sqrt{LC}} \quad \text{or} \quad f_n = \frac{1}{2\pi\sqrt{LC}} \tag{19}$$

$$2\delta\omega_n = \frac{R_s + Z_0/2}{L} \tag{20}$$

$$\delta = \frac{R_s + Z_0/2}{2L\omega_n} = \frac{R_s + Z_0/2}{2}\sqrt{\frac{C}{L}}. \tag{21}$$

Since we want to optimize the circuit bandwidth, consistent with an acceptable system real time response, the damping factor δ can be set equal to approximately 1/2 [16]. The system bandwidth and real time response will be determined by the circuit under consideration, the sampling pulse bandwidth limitations, the nonideality of the sampling diodes, and the physical realization of the sampling device. It is for this reason that we can set the damping factor of the input sampling circuit at 1/2 and yet achieve an acceptable real time response for the overall system, which corresponds to a damping factor of $1/\sqrt{2}$. Having established the damping factor, there are many combinations of R, L, and C that will yield bandwidths in excess of 15 GHz. (The bandwidth of the input sampling circuit must be in excess of 15 GHz for the resultant sampler bandwidth to be in excess of 12.4 GHz.)

Sensitivity or conversion loss is always of prime importance so the choice of R, L, and C must be made with this consideration in mind. For maximum sensitivity, we require minimum diode series resistance consistent with bandwidth, dynamic range, and physical realizability. Figure 8 shows the relative location of one complex pole (the conjugate pole is not shown) as a result of varying R, L, and C. The dashed lines represent damping factor contours for various values of δ. The bandwidth objective for the input sampling circuit can be achieved if the following set of element values can be realized:

$$Z_0 = 50 \text{ ohms} \tag{22}$$

$$L = 250 \text{ pH} \tag{23}$$

$$C = 0.2 \text{ pF} \tag{24}$$

$$R = 10 \text{ ohms}. \tag{25}$$

The resulting diode equivalent circuit element values are as follows:

$$R_s = 20 \text{ ohms} \tag{26}$$

$$C_j = 0.1 \text{ pF} \tag{27}$$

$$L_s < 500 \text{ pH}. \tag{28}$$

From (3) and (23) we see that the total sampling loop inductance per side must be less than 500 ph, which means that the single packaged diode series inductance must be less than this value. In practice, this total permissible loop inductance places very stringent requirements upon the mechanical realization of the sampling circuit.

B. Split-Ground Configuration

Having established the desired element values, we can see that the electrical constraints placed upon the basic circuit will not be easily achieved. The interconnection of the sampling pulse line and the sampling diodes is complicated by the requirement of a very low impedance connection between the grounds of the input signal and the sampling capacitor. The impedance of this connection is represented by inductor L_2 and resistor R_{s_g} in Fig. 4. The two-diode feedthrough sampling configuration shown in Fig. 9 yields the lowest impedance connection possible by making the grounds of the input signal and the sampling capacitor physically the same point. This is accomplished by splitting the ground of the input coaxial transmission line in order to develop an impedance from one side of ground to the other. The input and output to the sampling section, shown in dotted lines in Fig. 9, are coaxial lines. The transmission line between B and B' can take any one of several forms. A 50 Ω impedance must be maintained between the center conductor and the two ground planes. At the same time, the two ground planes, when driven in a balanced fashion, must have a finite impedance across which we can develop the sampling pulse. This means that two modes of transmission, which are electrically but not mechanically isolated from each other, will appear on the same transmission line. This split-ground

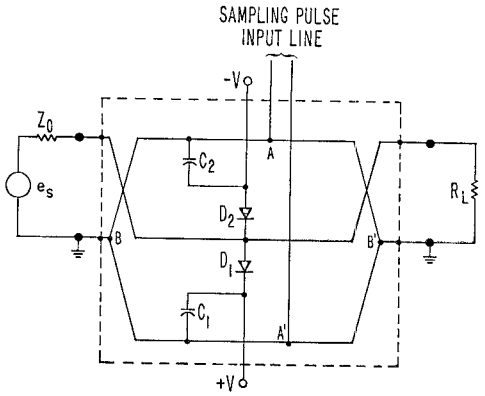

Fig. 9. Two diode feedthrough sampling circuit.

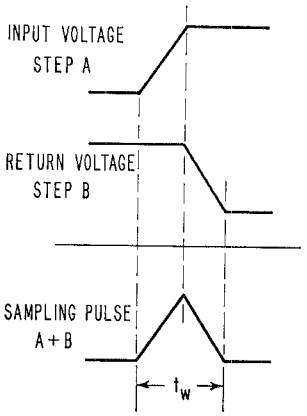

Fig. 10. Sampling pulse.

section provides an ideal entry point for the sampling signal, since it can now be applied to the ground of the RF transmission line and yet develop a sampling voltage. The RF transmission line center conductor can be ignored, since it lies on an equipotential plane with respect to the applied sampling voltage. The sampling signal can now take the form of a voltage step which will travel out the split-ground transmission line towards the shorts at B and B'. The voltage step will be inverted and travel back to the point AA'. A sampling voltage step supplied to the split-ground shorted stub transmission line will be transformed into a pulse, as shown in Fig. 10. The base width t_ω is related to the stub transmission line length as follows:

$$t_\omega = \frac{4d}{v}$$

d = one way distance from AA' to transmission line short.

v = velocity of propagation in the shorted transmission line.

Ideally, we would like to match the sampling pulse input line to the split-ground plane shorted stub. One particularly appealing form for this shorted stub is a biconical transmission line as shown in Fig. 11. In order to prevent the sampling voltage from being reflected

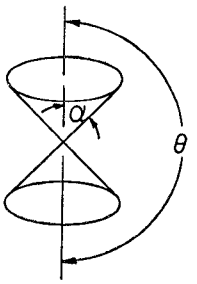

Fig. 11 Biconical transmission line.

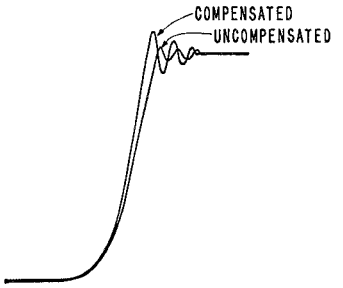

Fig. 12. Sampler real time step response.

before it arrives at the short, we want to maintain a constant impedance along the transmission line. The impedance of a biconical transmission line driven from its center is constant and is given by the following equation (see Reference [17]):

$$Z_0 = \frac{120}{\sqrt{\epsilon_r}} \cosh^{-1}\left[\frac{\sin\frac{\theta}{2}}{\sin\alpha}\right]. \tag{30}$$

We have already stated that we want to mask out the diode package capacity. This can be done by embedding the diode package in a dielectric filled transmission line. In the configuration under consideration, this means that the cavity should be dielectric filled. The dielectric medium used must have low loss and a dielectric constant which is relatively close to that of the diode package material. It is not necessary, however, to totally mask out both the package capacitance and the diode chip capacitance in order to achieve the objective bandwidth specification.

The unmasked diode capacitance, which appears at the sampling node, causes the voltage standing-wave ratio at the input to the sampling device to increase with increasing frequency. A sampling device of this type will be called an uncompensated sampler. Some applications of sampling require that the VSWR at the input to the device be held to a minimum at the expense of real time step response. This can be accomplished by incorporating the unmasked diode capacitance in a low-pass T-filter network. The voltage appearing at the center node of such a filter, as a result of an input voltage step, will have overshoot. Figure 12 shows the sampler real time step response for both the compensated and uncompensated samplers.

C. Biconical Sampling Configuration

The sampling circuit shown in Fig. 9 can be implemented as shown in Fig. 13. The input and output transmission lines have been stepped down in size through the use of a compensated three-section taper. (Only two of the three sections are shown.) Figure 13 shows an exploded cutaway view of the internal cavity geometry. It should be noted that a 50 ohm impedance is maintained throughout the sampling structure, except for the unmasked diode capacity at the sampling node. A shorted biconical transmission line (biconical cavity) is used as a pulse forming line in the generation of the sampling pulse. The conical faces are truncated to provide room for the diodes and the sampling pulse entry into the biconical cavity. The diodes shown by dotted lines in Fig. 13 give the location of the diodes when the cavity is assembled. The biconical cavity is driven from one side through a short section of microcoax transmission line.

The cavity is dielectric filled in order to mask out some of the diode capacity. The electrical length of the cavity from the center to the short is 25 picoseconds, so the round trip or differentiation length is 50 picoseconds. The RF transmission line being sampled lies on a zero-potential plane with respect to the sampling pulse, providing approximately 40 dB of isolation between the sampling pulse and the RF transmission line.

The diode being used is a specially designed hot carrier diode in a low capacitance, low inductance package. A hot carrier diode is particularly suited for this application due to its extremely fast response. The packaged hot carrier diode has equivalent circuit element values that are consistent with the design requirement already stated.

The sampling capacitors, which store the charge taken during each sample, are located at the diodes to ensure a low inductance sampling path from the RF transmission line, through the sampling capacitors, to ground. The low-pass filter network for the compensated sampler can be built into the biconical cavity by increasing the impedance of the feedthrough transmission line adjacent to the sampling diodes. This takes the form of a modified center conductor in the truncated section of the biconical cavity.

D. Test Configuration

The bandwidth of a sampling device can be measured using the test configuration of Fig. 14. The sampler is loaded at its output port and a CW signal is applied at the input. If a periodic sampling signal, unsynchronized with the CW signal, is applied at the sampling port, the output to the video amplifier will be a series of random samples of the input. If the repetition rate of the sampling signal is chosen properly, the random samples of the input can be combined in such a way that the monitored output v_0 will be

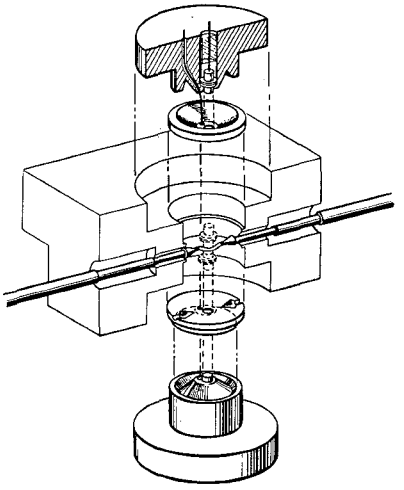

Fig. 13. Biconical sampling cavity.

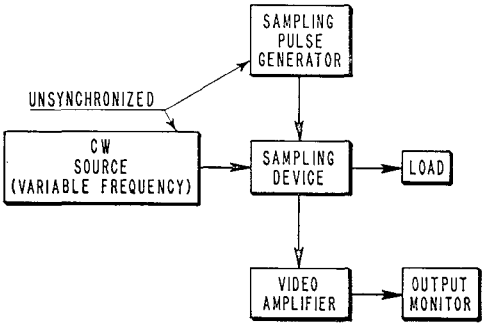

Fig. 14. Sampling test configuration.

$$V_0 = V_{in}\eta G, \tag{31}$$

where

V_{in} = input voltage,
η = sampling efficiency,
G = system gain.

If we now vary the frequency of the CW input signal while maintaining a constant peak-to-peak input voltage, we can plot η as a function of frequency by monitoring the output from the video amplifier. The bandwidth of the sampling device is defined to be that frequency where η is $1/\sqrt{2}$ times its dc or low-frequency value.

E. Tests Results

Sampling devices of the type described in this paper have been assembled and tested. Average experimental results for both the compensated and uncompensated samplers are shown in Fig. 15. These results were obtained using a sampling voltage step with a risetime of approximately 80 picoseconds.

The VSWR for the uncompensated sampler increases with frequency as a result of the unmasked diode capacity. The compensated sampler shows the predicted lower VSWR and increased high-frequency response.

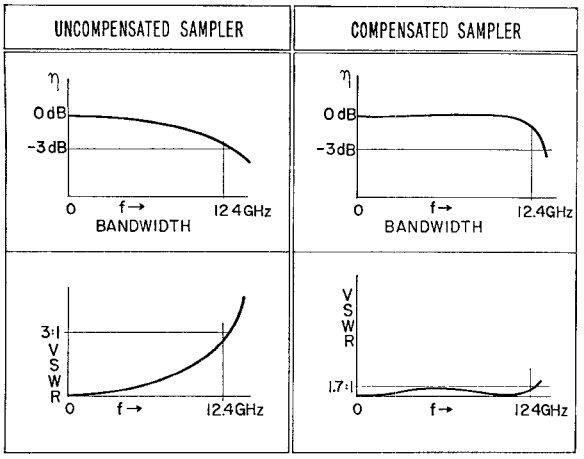

Fig. 15. Average measured performance.

Conclusion

The bandwidths obtained, using the electromechanical configuration just described, are well in excess of 12.4 GHz. This represents an increase in bandwidth of three to four times that previously available. It is safe to assume that this technique will eventually be used to achieve bandwidths in excess of 18 GHz.

Acknowledgment

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Theoretical and Practical Applications of Capacitance Matrix Transformations to TEM Network Design

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***Abstract*—TEM propagation on an array of parallel conductors is described in terms of the normalized static capacitance matrix. Important properties of capacitance matrices are discussed and a physical and network interpretation is given to a useful linear transformation of the static capacitance matrix. Several practical applications of capacitance matrix transformations are given. These include 1) equivalent circuits for directional couplers with equal terminations, 2) design procedures for directional couplers with unequal terminations, and 3) element value tables and design details for compact coaxial filter-transformers. Construction details and experimental results are presented for a 3:1 bandwidth filter-transformer constructed with multiple re-entrant coaxial lines.**

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I. Introduction

AN IMPORTANT ASPECT of TEM quarter-wave network synthesis and design is the multiplicity of physical configurations that yield iden-